REMARKS

Claims 1-43 remain pending. In the present Office Action, claims 1-3, 6-7, 12-17, 21-28, 32-33, 35-38, 40, and 42 were rejected under 35 U.S.C. § 102(b) as being anticipated by Bonke et al., U.S. Patent No. 5,812,564 ("Bonke"). Claims 4-5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Bonke in view of Yoshimura, U.S. Patent No. 5,848,076 ("Yoshimura"). Claims 8, 18-20, and 29-31 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Bonke. Claims 9-11, 34, and 39 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Bonke in view of Hetherington, U.S. Patent No. 4,995,041 ("Hetherington"). Claims 41 and 43 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Agarwal, U.S. Patent No. 6,477,669 ("Agarwal"). Applicants respectfully traverse these rejections and request reconsideration.

Claims 1-43 are Patentable over the Cited Art

Applicants respectfully submit that claims 1-43 are patentable over the cited art. The present Office Action essentially maintains the art rejections from the previous Office Action, updating the rejection for the newly-added dependent claims, with the exception of the Agarwal rejection discussed below. Applicants believe that the remarks from the Response to Office Action filed July 16, 2004 (and received in the PTO on July 19, 2004, according to the present Office Action, referred to herein as the "previous Response") illustrate reasons why claims 1-43 are patentable over the cited art. Applicants incorporate the remarks from the previous Response herein by reference to preserve them for appeal. Applicants respond to the Response to Arguments section of the present Office Action below.

The present Office Action alleges that the microcontroller 200 is capable of posting error information to the microprocessor 34 to initiate a read retry, and therefore concludes that Bonke teaches the microcontroller 200 executes a first instruction which causes an access to first data in a memory. See Office Action, page 2, last paragraph, referring to Bonke, col. 28, lines 44-54. The cited section of Bonke refers to posting the error to the microprocessor 34 for a possible read retry after the error has been detected as

uncorrectable. These teachings do not teach or suggest "execution circuitry configured to execute a first instruction which causes *an access to first data* in a memory; an error correction code (ECC) check circuit configured to detect an ECC error *in response to the access to the first data* in the memory; and a microcode unit coupled to receive an indication that the ECC check circuit has detected the ECC error, wherein the microcode unit, in response to the indication, is configured to dispatch a microcode routine ...the execution circuitry is further configured to execute the instructions in the microcode routine" as recited in claim 1. As highlighted in the previous Response, the accesses in Bonke which cause errors to be detected and which cause the microcontroller 200 to execute its error handling microcode are host-generated accesses (see Bonke, description of Fig. 1).

Bonke teaches: "If in any of the above-noted error correction calculations the error is deemed uncorrectable, operations may be halted and the error optionally posted to microprocessor 34. If the error is posted to microprocessor 34 it may determine whether a read retry of the data should be attempted, whether other correction procedures are to be performed, whether to send uncorrected data to the host, or whether the read should be aborted and an error corrector error should be immediately posted to the host. The microprocessor may also perform erasure correction using other erasure information for the read data." (Bonke, col. 28, lines 44-54). Thus, it is clear that the microcontroller 200 posting the error to the microprocessor 34 and the microprocessor 34 attempting a read retry of the data are all performed in response to determining that a previously detected error is uncorrectable. Particularly, the previously detected error is detected during a host-generated operation. ***There is no teaching that the microcontroller 200's error handling microcode is invoked in response to an error during a read retry initiated by the microprocessor 34.*** Furthermore, it would appear that if Bonke's read retry were to invoke the error handling microcode in the microcontroller 200, the error would again be uncorrectable, causing another post to the microprocessor 34 and another read retry. Thus, Bonke's system would be in an infinite loop, not making forward progress. For at least the above reasons, Applicants submit that there is no teaching in Bonke that any instruction executed by the microcontroller 200 causes an access to data

during which a detection of an error in response to that access causes the microcontroller 200 to execute its error handling microcode.

For at least the above stated reasons, Bonke does not teach or suggest "execution circuitry configured to execute a first instruction which causes an access to first data in a memory; an error correction code (ECC) check circuit configured to detect an ECC error in response to the access to the first data in the memory; and a microcode unit coupled to receive an indication that the ECC check circuit has detected the ECC error, wherein the microcode unit, in response to the indication, is configured to dispatch a microcode routine ...the execution circuitry is further configured to execute the instructions in the microcode routine" as recited in claim 1. Applicants submit that claim 1 is patentable over the cited art. Claims 2-22 depend from claim 1, and thus are patentable over the cited art for at least the above stated reasons as well. Each of claims 2-22 recite additional combinations of features not taught or suggested in the cited art. **In view of the remarks above illustrating the patentability of claim 1 over the cited art, additional remarks regarding the additional features in claims 2-22 are deemed unnecessary at this time. However, Applicants reserve the right to present such additional remarks on appeal.**

Claim 23 recites a combination of features including: "a microcode unit coupled to receive an indication of an error correction code (ECC) error for first data, wherein the microcode unit, in response to the indication, is configured to dispatch a microcode routine stored by the microcode unit, wherein the microcode routine includes instructions which, when executed, correct the ECC error; and execution circuitry coupled to receive the instructions from the microcode unit, wherein the execution circuitry is configured to execute the instructions, and wherein the execution circuitry is also configured to execute a first instruction that causes an access to the first data in the memory, wherein the ECC error is detected during the access". The same teachings related to Bonke's microcontroller 200 discussed above are alleged to teach the above highlighted features of claim 23. Applicants respectfully submit that, for reasons similar to those highlighted

above with regard to claim 1, Bonke's microcontroller 200 fails to teach or suggest the above highlighted features of claim 23 as well.

For at least the above stated reasons, Applicants submit that claim 23 is patentable over the cited art. Claims 24-34 and 39-43 depend from claim 23, and thus are patentable over the cited art for at least the above stated reasons as well. Each of claims 24-34 and 39-43 recite additional combinations of features not taught or suggested in the cited art. **In view of the remarks above illustrating the patentability of claim 23 over the cited art, additional remarks regarding the additional features in claims 24-34 and 39-43 are deemed unnecessary at this time. However, Applicants reserve the right to present such additional remarks on appeal.**

Claim 35 recites a combination of features including: "performing an access to first data in a memory in response to executing a first instruction in execution circuitry; detecting an ECC error in response to the access; and dispatching a microcode routine stored by a microcode unit in response to the detecting, wherein the microcode routine includes instructions which, when executed in the execution circuitry, correct the ECC error in the memory". Applicants respectfully submit that Bonke's microcontroller 200 does not teach or suggest the above highlighted features either, for reasons similar to those highlighted above.

For at least the above stated reasons, Applicants submit that claim 35 is patentable over the cited art. Claims 36-38 depend from claim 35, and thus are patentable over the cited art for at least the above stated reasons as well. Each of claims 36-38 recite additional combinations of features not taught or suggested in the cited art. **In view of the remarks above illustrating the patentability of claim 35 over the cited art, additional remarks regarding the additional features in claims 36-38 are deemed unnecessary at this time. However, Applicants reserve the right to present such additional remarks on appeal.**

Agarwal Reference/Rejection

Applicants note that Agarwal does not appear to be of record in the present application, as it is not listed on a PTO-1449 form nor on a PTO-892 form. Applicants respectfully request that the Examiner issue a PTO-892 form with the next action listing the Agarwal reference.

Additionally, Applicants note that the Agarwal rejection fails to form a *prima facie* case of obviousness of claims 41 and 43. Claims 41 and 43 depend from claim 40, which depends from claim 23. Thus, for Agarwal to form a *prima facie* case of obviousness of claims 41 and 43, Agarwal must teach or suggest all of the features of claims 40 and 23, also. The Office Action makes no attempt to illustrate why Agarwal allegedly teaches the features of claims 40 and 23.

Furthermore, the rejection refers to the computer system on which one is typing as evidence of modems/audio devices being allegedly common. Applicants note that the computer system on which one is currently typing is not a valid analysis under section 103, as the computer system on which one is currently typing may not have existed at the time the invention was made.

CONCLUSION

Applicants submit that the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-75900/LJM.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☐ Petition for Extension of Time

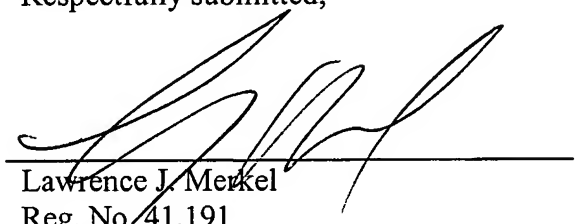
☐ Request for Approval of Drawing Changes

☐ Notice of Change of Address

☐ Fee Authorization Form authorizing a deposit account debit in the amount of $ for fees ( ).

☐ Other:

Respectfully submitted,



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